CLAIMS

What is claimed is:

1. A method comprising:

a) receiving a plurality of symbols in a first integrated circuit (IC) device, the symbols having been transmitted by a second IC device and received over a serial point to point link, wherein the plurality of symbols include a non-data sequence inserted according to a predetermined methodology into a data sequence by the second IC device;

b) loading the plurality of symbols into a buffer according to a load pointer;

c) unloading the data sequence and some of the non-data sequence from the buffer according to a changing unload pointer that points to different entries of the buffer, wherein the unload pointer is changed by one entry each time a symbol is unloaded; and

d) to prevent overflow of the buffer, and in response to (i) detecting the non-data sequence at an inlet of the buffer and (ii) passing an indicator that refers to such detection through the buffer, changing the unload pointer by more than one entry so that a non-data symbol of the non-data sequence, as loaded in the buffer, is skipped while unloading in c).

2. The method of claim 1 wherein the non-data sequence is detected by detecting a combination of a first non-data symbol followed by a second, different non-data symbol in said non-data sequence.

3. The method of claim 2 wherein the passing of the indicator comprises generating a flag in response to detecting the first and second non-data symbols of said non-data sequence, and aligning the flag with the first non-data symbol when loading the flag with said non-data sequence into the buffer in b).

4. The method of claim 3 wherein the unload pointer is changed in d) in response to detecting the flag at an outlet of the buffer, so that the second non-data symbol, as loaded in the buffer, is skipped.

5. The method of claim 1 wherein the non-data sequence is a PCI Express sequence that includes the non-data symbol COM followed by the non-data symbol SKP.

6. A method comprising:

a) receiving a plurality of symbols in a first integrated circuit (IC) device, the symbols having been transmitted by a second IC device and received over a serial point to point link that couples the first and second IC devices, wherein the plurality of symbols include a non-data sequence inserted into a data sequence by the second IC device;

b) loading the plurality of symbols into a buffer according to a load pointer;

c) unloading the data sequence and some of the non-data sequence from the buffer according to a changing unload pointer, wherein the unload pointer is changed by one entry of the buffer each time a symbol is unloaded; and

d) to prevent underflow of the buffer, and in response to (i) detecting the non-data sequence at an inlet of the buffer and (ii) passing an indicator that refers to such detection through the buffer, stalling the unload pointer at an entry of the buffer that contains a non-data symbol while unloading in c).

7. The method of claim 6 wherein the non-data sequence is detected by detecting a combination of a first non-data symbol followed by a second, different non-data symbol in said non-data sequence.

8. The method of claim 7 wherein the passing of the indicator comprises:

generating a flag in response to detecting the first and second non-data symbols of said non-data sequence, and aligning the flag with the first non-data symbol when loading said non-data sequence into the buffer in b).

9. The method of claim 8 wherein the unload pointer is stalled, in response to detecting the flag at an outlet of the buffer, at an entry of the buffer that contains the second non-data symbol of the non-data sequence.

10. The method of claim 6 wherein the non-data sequence is a PCI Express sequence that includes the non-data symbol COM followed by the non-data symbol SKP.

11. An integrated circuit (IC) device comprising:

a buffer having an input to receive a plurality of symbols that were transmitted by another IC device over a serial point to point link, the buffer having a plurality of entries;

detect logic having an input to receive the plurality of symbols and an output to feed the input of the buffer a non-data symbol sequence identifier;

first pointer logic to provide a first pointer to sequentially load the plurality of symbols into the plurality of entries of the buffer, respectively;

second pointer logic to provide a second pointer to sequentially unload the plurality of symbols from the plurality of entries of the buffer, respectively;

comparison logic to compare the first and second pointers; and

pointer control logic having an output coupled to the second pointer logic,

wherein the pointer control logic is to stall the second pointer at an entry that contains a non-data symbol, in response to a) said identifier appearing at the output of the buffer, and b) the comparison logic indicating that the buffer is less full than a predetermined threshold.

12. The IC device of claim 11 wherein the plurality of symbols are to be received in accordance with a first clock signal which is to be derived from a transmit clock of said another IC device.

13. The IC device of claim 12 wherein the first clock signal is to be derived from the transmit clock being embedded in a stream of information that contains the plurality of symbols and is to be transmitted by said another IC device.

14. The IC device of claim 12 wherein the second pointer logic is to advance the second pointer in accordance with a second clock signal that is derived from a local clock of the IC device,

and wherein the first pointer logic is to advance the first pointer in accordance with the first clock signal.

15. A system comprising:

a processor;

a main memory; and

an integrated circuit (IC) device which is communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device having link interface circuitry that supports a serial, point to point link, the circuitry includes

a buffer having an input to receive a plurality of symbols that were transmitted over the link, the buffer having a plurality of entries,

detect logic having an input to receive the plurality of symbols and an output to feed the input of the buffer a non-data symbol sequence identifier,

first pointer logic to provide a first pointer to load the plurality of symbols into the plurality of entries of the buffer, respectively,

second pointer logic to provide a second pointer to sequentially unload the plurality of symbols from the plurality of entries of the buffer,

comparison logic to compare the first and second pointers, and

pointer control logic having an output coupled to the second pointer logic, wherein the pointer control logic is to stall the second pointer at an entry that contains a non-data symbol, in response to a) said identifier appearing at the output of the buffer, and b) the comparison logic indicating that the buffer is less full than a predetermined threshold.

16. The system of claim 15 wherein the plurality of symbols are to be received in accordance with a first clock signal which is to be derived by the IC device from a transmit clock of another device.

17. The system of claim 16 wherein the first clock signal is to be derived from the transmit clock being embedded in a stream of information that contains the plurality of symbols and is to be transmitted by said another device.

18. The system of claim 16 wherein the second pointer logic is to advance the second pointer in accordance with a second clock signal that is derived from a local clock of the root complex,

and wherein the first pointer logic is to advance the first pointer in accordance with the first clock signal.

19. The system of claim 15 further comprising a graphics element; and

wherein the IC device is a memory controller hub (MCH) that communicatively couples the processor to the main memory and the graphics element.

20. The system of claim 15 wherein the IC device is an I/O controller hub (ICH) that communicatively couples the processor to peripheral devices.

21. A method for buffer management, comprising:

detecting a predefined non-data symbol sequence at an inlet of an elastic buffer;

passing an identifier that represents detection of said sequence through the elastic buffer; and

processing the identifier at an outlet of the elastic buffer to avoid one of overflow and underflow conditions in the elastic buffer.

22. The method of claim 21 wherein the sequence is a PCI Express SKP Ordered Set.

23. The method of claim 21 wherein the processing is designed to maintain the elastic buffer in a half-full state.

24. An integrated circuit (IC) device comprising:

a buffer having an input to receive a plurality of symbols that were transmitted by another IC device over a serial point to point link, the buffer having a plurality of entries;

detect logic having an input to receive the plurality of symbols and an output to feed the input of the buffer a non-data symbol sequence identifier;

first pointer logic to provide a first pointer to sequentially load the plurality of symbols into the plurality of entries of the buffer, respectively;

second pointer logic to provide a second pointer to sequentially unload the plurality of symbols from the plurality of entries of the buffer, respectively;

comparison logic to compare the first and second pointers; and

pointer control logic having an output coupled to the second pointer logic, wherein the pointer control logic is to advance the second pointer by more than one entry to skip over an entry that contains a non-data symbol, in

response to a) said identifier appearing at the output of the buffer, and b) the comparison logic indicating that the buffer is more full than a predetermined threshold.

25. The IC device of claim 24 wherein the plurality of symbols are to be received in accordance with a first clock signal which is to be derived from a transmit clock of said another IC device.

26. The IC device of claim 25 wherein the first clock signal is to be derived from the transmit clock being embedded in a stream of information that contains the plurality of symbols and is to be transmitted by said another IC device.

27 The IC device of claim 25 wherein the second pointer logic is to advance the second pointer in accordance with a second clock signal that is derived from a local clock of the IC device, and wherein the first pointer logic is to advance the first pointer in accordance with the first clock signal.

28. A system comprising:

a processor;

a main memory; and

an integrated circuit (IC) device which is communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device having link interface circuitry that supports a serial, point to point link, the circuitry includes

a buffer having an input to receive a plurality of symbols that were transmitted over the link, the buffer having a plurality of entries,

detect logic having an input to receive the plurality of symbols and an output to feed the input of the buffer a non-data symbol sequence identifier,

first pointer logic to provide a first pointer to load the plurality of symbols into the plurality of entries of the buffer, respectively,

second pointer logic to provide a second pointer to sequentially unload the plurality of symbols from the plurality of entries of the buffer,

comparison logic to compare the first and second pointers, and

pointer control logic having an output coupled to the second pointer logic, wherein the pointer control logic is to advance the second pointer by more than one entry to skip over an entry that contains a non-data symbol, in response to a) said identifier appearing at the output of the buffer, and b) the comparison logic indicating that the buffer is more full than a predetermined threshold.

29. The system of claim 28 wherein the plurality of symbols are to be received in accordance with a first clock signal which is to be derived by the IC device from a transmit clock of another device.

30. The system of claim 29 wherein the first clock signal is to be derived from the transmit clock being embedded in a stream of information that contains the plurality of symbols and is to be transmitted by said another device.

31. The system of claim 29 wherein the second pointer logic is to advance the second pointer in accordance with a second clock signal that is derived from a local clock of the root complex,

and wherein the first pointer logic is to advance the first pointer in accordance with the first clock signal.

32. The system of claim 28 further comprising a graphics element; and

wherein the IC device is a memory controller hub (MCH) that communicatively couples the processor to the main memory and the graphics element.

33. The system of claim 28 wherein the IC device is an I/O controller hub (ICH) that communicatively couples the processor to peripheral devices.